322D7881

FROM CONTROL

10 COUNT IN STORE

A-6C

11 STORE SCR

A-6F

12 MULTIPLY

A-6G

13 DIVIDE

100 MATRIX ADDRESS: S0 $\overline{S4}$ DC DG

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J.reg. then read number from that address into M.reg.	MTF	*
	DTF_1	*
	DTF_2	*
	DTG	T1
	VTG	T2
	DTM	T3
	GTJ	T4
	READ	*

101 MATRIX ADDRESS: S1 $\overline{S4}$ DC DG

OPERATION	WAVE-FORMS	TIMING
Increase number in M.reg. by 1 then write the increased number back into store.	MTF	*
	ITF	*
	DTG	T1
	FTG	T2
	DTM	T3
	GTM	T4
	WRITE	*

110 MATRIX ADDRESS: S0 DA DG

OPERATION	WAVE-FORMS	TIMING
Transfer address of storing location from M.reg. into Q.reg. and set J.reg. with address of SCR then read contents of SCR into M.reg.	MTF	*
	DTF_1	*
	DTF_2	*
	ETJ	*
	DTG	T1
	VTG	T2
	DTQ	T3
	DTM	T3
	GTQ	T4
	READ	*
	WRITE	*

111 MATRIX ADDRESS: S1 DA DG

OPERATION	WAVE-FORMS	TIMING
Transfer address from Q.reg. into J.reg.	DTF	*
	DTG	T1
	FTG	T2
	DTJ	T3
	GTJ	T4

112 MATRIX ADDRESS: S2 DA DG

OPERATION	WAVE-FORMS	TIMING
Place top 5 digits of M.register into Q. register.	MTF	*
	DTF_2	*
	DTG	T1
	VTG	T2
	DTQ	T3
	GTQ	T4

113 MATRIX ADDRESS: S3 DA DG

OPERATION	WAVE-FORMS	TIMING
Clear top 5 digits of M.register and write into address in J. reg.	MTF	*
	DTF_1	*
	DTG	T1
	VTG	T2
	DTM	T3
	GTM	T4
	CLEAR	*
	WRITE	*

120 MATRIX ADDRESS: S0 $\overline{S4}$ DD DE

OPERATION	WAVE-FORMS	TIMING
Transfer address from M. reg. into J.reg. then read contents of that address into M. reg.	MTF	*
	DTG	T1
	FTG	T2
	DTM	T3
	GTJ	T4
	READ	*
	WRITE	*

121 MATRIX ADDRESS: S1 $\overline{S4}$ DD DE

OPERATION	WAVE-FORMS	TIMING
Transfer A.reg. into Q.reg. then set up count of 17 in P.C. Set A.reg. and X overflow to zero. Compare X with Q1.	ATF	*
	KTJ	*
	TXQ1	*
	DTG	T1
	FTG	T2
	DTA	T3
	DTJ	T3
	DTQ	T3
	DTX	T3
	GTQ	T4
	JTPC	T5

X=Q1 — **122C** MATRIX ADDRESS: S2 $\overline{S4}$ DD DE CC

OPERATION	WAVE-FORMS	TIMING
Right shift A reg. 1 place and set X with overflow. Decrease count in P.C. by 1.	ATF	*
	VTX	*
	DTG	T1
	RTG	T2
	DTA	T3
	DTX	T3
	ITPC	T4
	GTA	T4

$X\overline{Q1}$ — **122A** MATRIX ADDRESS: S2 $\overline{S4}$ DD DE CA

OPERATION	WAVE-FORMS	TIMING
Add A.reg. to M.reg. then right shift 1 place and place result in A. reg. and overflow in X. Decrease count in P.C. by 1.	ATF	*
	MTF	*
	VTX	*
	DTG	T1
	RTG	T2
	DTA	T3
	DTX	T3
	ITPC	T4
	GTA	T4

$\overline{X}Q1$ — **122B** MATRIX ADDRESS: S2 $\overline{S4}$ DD DE CB

OPERATION	WAVE-FORMS	TIMING
Subtract M. reg. from A. reg. then right shift 1 place and place result in A.reg. and overflow in X. Decrease count in P.C. by 1.	ATF	*
	MTF	*
	ITF	*
	VTX	*
	DTG	T1
	RTG	T2
	DTA	T3
	DTX	T3
	ITPC	T4
	GTA	T4

124 MATRIX ADDRESS: S0 S4 DD DE

OPERATION	WAVE-FORMS	TIMING
Right shift Q reg. by 1 place and add X1 (to Q18) then place result in Q. reg. and overflow in X Test PC for 0 Compare X with Q1.	DTF	*
	XTF	*
	VTX	*
	TPCO	*
	DTG	T1
	RTG	T2
	DTX	T3
	DTQ	T3
	GTQ	T4
	TXQ1	*

C≠0

X=Q1 — **123C** MATRIX ADDRESS: S3 S4 DD DE CC

OPERATION	WAVE-FORMS	TIMING
Set X to zero	DTX	T3

C=0 $X\overline{Q1}$ — **123A** MATRIX ADDRESS: S3 $\overline{S4}$ DD DE CA

OPERATION	WAVE-FORMS	TIMING
Add A.reg. to M.reg. and place result in A.reg. Set X to zero.	ATF	*
	MTF	*
	DTG	T1
	FTG	T2
	DTA	T3
	DTX	T3
	GTA	T4

$\overline{X}Q1$ — **123B** MATRIX ADDRESS: S3 $\overline{S4}$ DD DE CB

OPERATION	WAVE-FORMS	TIMING
Subtract M. reg. from A.reg. and place result in A.reg. Set X to zero	ATF	*
	MTF	*
	ITF	*
	DTG	T1
	FTG	T2
	DTA	T3
	DTX	T3
	GTA	T4

130 MATRIX ADDRESS: S0 $\overline{S4}$ DB DE

OPERATION	WAVE-FORMS	TIMING
Transfer address from M.reg. into J. reg. then read contents of that address into M.reg.	MTF	*
	DTG	T1
	FTG	T2
	DTM	T3
	GTJ	T4
	READ	*
	WRITE	*

131 MATRIX ADDRESS: S1 $\overline{S4}$ DB DE

OPERATION	WAVE-FORMS	TIMING
Right shift Q. reg. by 1 place and place result in Q. reg. Set J. reg. to zero.	DTF	*
	DTG	T1
	RTG	T2
	DTQ	T3
	DTJ	T3
	GTQ	T4

132 MATRIX ADDRESS: S2 $\overline{S4}$ DB DE

OPERATION	WAVE-FORMS	TIMING
Left shift Q. reg. by 1 place and set up count of 18 in P.C.	QTF	*
	KTJ	*
	K2	*
	DTG	T1
	LTG	T2
	DTQ	T3
	GTQ	T4
	JTPC	T5

133 MATRIX ADDRESS: S3 $\overline{S4}$ DB DE

OPERATION	WAVE-FORMS	TIMING
Left shift A. reg. 1 place whilst transferring to G.reg. Set X with overflow. Test XM18.	ATF	*
	VTX	*
	DTG	T1
	LTG	T2
	DTX	T3
	TXM18	*

X=M18 — **134B** MATRIX ADDRESS: S0 S4 DB DE $\overline{CA}$

OPERATION	WAVE-FORMS	TIMING
Add 1 to Q.reg. then left shift by 1 place. Set X with overflow. Decrease count in PC by 1. Retain setting at conditionals.	QTF	*
	ITF	*
	VTX	*
	CRS	*
	DTG	T1
	LTG	T2
	DTX	T3
	DTQ	T3
	GTQ	T4
	ITPC	T4

134A $X\neq M18$ MATRIX ADDRESS: S0 S4 DB DE CA

OPERATION	WAVE-FORMS	TIMING
Left shift Q. reg. by 1 place Set X with overflow. Decrease count in P.C. by 1. Retain setting at conditionals.	QTF	*
	VTX	*
	CRS	*
	DTG	T1
	LTG	T2
	DTX	T3
	DTQ	T3
	GTQ	T4
	ITPC	T4

PC≠0

136B MATRIX ADDRESS: S2 S4 DB DE $\overline{CA}$

OPERATION	WAVE-FORMS	TIMING
Subtract M. reg. from A. reg. then left shift by 1 place and add Xo then place result in A.reg. Set X with overflow. Test PC for zero. Compare X and MT8.	ATF	*
	MTF	*
	ITF	*
	XTF	*
	VTX	*
	TPCO	*
	DTG	T1
	LTG	T2
	DTA	T3
	DTX	T3
	GTA	T4
	TXM18	*

PC=0

136A MATRIX ADDRESS: S2 S4 DB DE CA

OPERATION	WAVE-FORMS	TIMING
Add A.reg. to M.reg then left shift by 1 place and add Xo then place result in A.reg. Set X with overflow. Test P.C. for zero. Compare X and M18	ATF	*
	MTF	*
	XTF	*
	VTX	*
	TPCO	*
	DTG	T1
	LTG	T2
	DTA	T3
	DTX	T3
	GTA	T4
	TXM18	*

PC=0

135 MATRIX ADDRESS: S1 S4 DB DE

OPERATION	WAVE-FORMS	TIMING
Add round off constant (1) to Q.reg. then transfer Q.reg. to A.reg.	QTF	*
	ITF	*
	DTG	T1
	FTG	T2
	DTA	T3
	GTA	T4

TO CONTROL

* Waveforms set true at T6 of previous timing cycle and set false at T6 of present timing cycle. Note that the waveforms CLEAR, READ, WRITE and some test waveforms (e.g. TM_{18}) whilst being set true at T6 of previous timing cycle are not in fact used until T5 of present timing cycle.

TITLE: 920 B CONTROL SEQUENCE FUNCTIONS 10-15

SHEET 1 OF 2

A12

LATEST MI INCORPORATED; MI 2998

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TITLE: 920B CONTROL SEQUENCE FUNCTIONS 10-15

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